



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Murphy Docket No: TI-33108
Serial No: 09/682,166 Examiner: Gonzalez, Jr.
Filed: 7/30/2001 Art Unit: 2834
For: ADJUSTABLE COMPENSATION OF A PIEZO DRIVE AMPLIFIER
DEPENDING ON MODE AND NUMBER OF ELEMENTS DRIVEN

APPEAL BRIEF PURSUANT TO 1.192(c)

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, PO Bx 1450, Alexandria, VA 22313-1450 on

5-26-04

Tommie Chambers
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The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed October 30, 2003, and the Advisory Action mailed March 5, 2004.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-43 were originally filed with Claims 9 and 43 standing cancelled. Thus, the subject matter of the instant appeal is the final rejection of Claims 1-8 and 10-42.

STATUS OF AMENDMENTS

The application was originally filed with Claim 1-43. By virtue of an amendment filed July 14, 2003, Appellants had cancelled Claims 9 and 43. Additionally, an Amendment After Final was filed on January 14, 2004, amending several claims. The Advisory Action indicated that the proposed amendment would not be entered.

SUMMARY OF THE INVENTION

Figure 1 is a block diagram of a generic disk drive system 10.

Figure 2 is an electrical schematic diagram of a portion of the positioning driver circuit 32, illustrating the overall structure of a milli-actuator circuit 40.

The milli-actuator driver circuitry 40 includes two operational transconductance amplifiers (OTAs) stages 44 and 46 to provide milli-actuator driving output signals to control an associated piezo element 48 through an external mirror circuit 50. The output from amplifier 44 is connected to the input of amplifier 46 by line 45. It should be noted that although the piezo element 48 may have a number of positioning elements in practice, only a single element is shown in the drawings for convenience. As will become apparent, the circuit 40 selectively provides either voltage mode or charge mode control of the milli-actuator. The input to the first stage amplifier 44 may be, for example, on lines 47 and 49 from a digital to analog converter (not shown) driven by the DSP 30 to control the piezo element of the milli-actuator.

The first OTA 44 is preferably operated in Class A mode, while the second OTA 46 is preferably operated in Class AB mode. The output of the second OTA 46 has three outputs, below described in detail, which provide a 1X output 52 to the sense capacitor 58 in charge mode, and two nX outputs 54 and 56 to the external current mirror 50 in voltage mode. The multiple "n" of the nX outputs may be as needed for the particular application; for example, in one embodiment n may be 10 to provide a 10X output, and in another embodiment, n may be 6.125 to provide a 6.125X output.

A decoder 51 is provided to decode signals indicating the desired mode of operation of the milli-actuator driving circuit 40, as well as the number of piezo elements that are being driven. The data may be provided, for example, from data that is inputted to the serial port (not shown) of the mass data storage device, to be decoded by the decoder 51. In a preferred embodiment, the decoder 51 may be, for example, merely a memory element into which configuration data is held from the initializing serial port data provided by the mass data storage device manufacturer.

The current or voltage mode of the circuit is controlled by a mode selection circuit 61 that includes two MOS transistors 60 and 62, which have a selection signal from the decoder 51 applied to their respective gates on lines 64 and 66. Thus, when driving the piezo motor in voltage mode, the 1X output 52 of the OTA 46 is disabled and the nX output 54 is used to create a voltage feedback loop through MOS transistor 62. In charge mode, MOS transistor 60 conducts, coupling the nX output 54 to analog ground, AGND 72. Also, in current mode, signals are provided on control lines 53 to the Class A amplifier 44 to control its impedance, as below described in detail.

In charge mode operation, a voltage feedback loop is formed with the 1X output driving the external sense capacitor 58, and the piezo element 48 is driven by the nX outputs 54 and 56. The charge delivered to the piezo element is determined by the ratio of the capacitance of the piezo element and the sense capacitance, the nX current drive ratio, and the voltage applied to the OTA 46 from the voltage source VM 72. The voltage source VM is referenced to analog ground 74.

With reference now additionally to Figures 3A-B, a detailed schematic of the amplifier 46 is shown.

The circuit 46 includes a shut-off circuit 84 that turns off the 1X output and drives it to a high impedance, for example, when the circuit is operated in voltage mode. A calibration circuit 86, as shown, provides inputs to the circuit 46 on lines 92 and 94. The 1X output is provided on output line 52 by pull-up and pull-down transistors 88 and 90, which are constructed in wells 96 and 98 that are connected respectively to AGND and VM. Outputs to the nX driver circuits, shown in detail in Figure 3B, are provided in voltage mode of operation on output lines 110 and 112.

With reference additionally now to Figure 3B, the details of the nX amplifiers 104 and 106 and the remaining calibration circuitry 108 are shown. It should be noted that the voltage of the nX amplifiers 104 and 106 may be other than the voltage VM of the 1X amplifier; however, they are also referenced to the analog ground potential, AGND.

Details of the Class A amplifier 44 are shown in the electrical schematic diagram of Figures 4A-B, to which reference is now additionally made.

To this end, the amplifier 44 receives control signals from the decoder 51 on lines 53 to control the impedance of the circuit. More particularly, the circuit 44 includes three chains 122, 124, and 126 of diode connected MOSFETs to establish the high-end impedance of the circuit. Chain 122 is normally on to set an nominal initial impedance or load, and chains 124 and 126 may be selectively turned on by initialization signals from the decoder 120 via respective amplifiers 128 and 130 to compensate for the largest anticipated gain of the circuit. Thus, for example, a typical impedance range of a Class A amplifier of the type described is between about 39 Kohms and 150 Kohms. The high-end range is determined by the combination of the changes 122, 124, and 126 by control signals on lines 53.

Additionally, with reference particularly to Figure 4A, the input differential amplifier 132 receives the input signals INM and INP on respective lines 47 and 49. Normally load transistors 134 and 136 are provided on the respective source and drain sides of the amplifier 132. By control signals on lines 53 from the decoder 51, however, additional load circuits 138-141 may be selectively connected in parallel with the normal load transistors 134 and 136. Thus, the impedance of the amplifier 44 may be widely controlled, in dependence on the control signals provided on lines 53.

ISSUES

The four issues on appeal are first whether Claims 3, 21, 29, and 37 are unpatentable under 35 U.S.C. § 112, second paragraph; second whether Claims 1, 6-8, 19, 24-27, 32-35, and 40-42 are unpatentable over Fontanella, Hanks, and Murray; third whether Claims 2, 3, 5, 20, 21, 23, 28, 29, 31, 36, 37, and 39 are unpatentable over Fontanella, Hanks, and Murray in view of Sullivan; and fourth whether Claims 4, 22, 30, and 38 are unpatentable over Fontanella, Hanks, Sullivan, and Liu.

GROUPING OF THE CLAIMS

Each of Claims 1, 10, 19, 27, and 35 are as contained in the attached Appendix are independently patentable, and these rejected claims do not stand or fall together for the reasons more clearly set forth herein below.

ARGUMENTS

Concerning the rejection under 35 U.S.C. § 112, second paragraph, Applicants have submitted a proposed amendment with the Amendment After Final to correct the concerns of the Examiner. However, the Examiner has refused to enter the amendment. However, once the Examiner enters the amendment it is respectfully submitted that this rejection is overcome.

It is respectfully submitted that Claims 1-8 and 10-42 are in full compliance with 35 U.S.C. § 112 and particularly points out and distinctly claims the subject matter which Appellants believe is their invention.

It is respectfully submitted that Fontanella does not disclose or suggest the presently claimed invention including the driving circuit for selectively driving the piezoelectric element in either a voltage mode or charge mode in independent Claim 1, a class AB amplifier connected to receive the output from the class A amplifier to selectively provide either a current mode driving signals or voltage mode driving signals to the piezo element in independent Claim 10, the step of selectively driving the piezo element in either the voltage mode or the charge mode in independent Claim 19, the means for selectively driving the piezo element in either a voltage mode or a charge mode in independent Claim 27 albeit defined as a driving circuit for selectively driving the piezo element in either a voltage mode or charge mode in independent Claim 35.

Applicants agree with the Examiner that Fontanella does not disclose that the piezo element may be driven in a voltage mode or in a charge mode as evidence by the top of Page 3 of the Final Office Action.

Hanks does not disclose or suggest the presently claimed invention including the driving circuit for selectively driving the piezo element in either a voltage mode or a charge mode as defined in the various forms in independent Claims 1, 10, 19, 27, and 35.

The Examiner alleges that Hanks discloses that a piezoelectric element may be driven in a voltage mode referring to Figure 4 or the charge mode referring for Figure 5.

However, Hanks does not disclose a single circuit for selectively driving the piezoelectric in either a voltage mode or the charge mode.

The circuits of Figure 4 and Figure 5 are separate embodiments.

Additionally, whether Murray discloses avoiding unwanted energy absorption and whether one of ordinary skill in the art would consider modifying Hanks or Fontanella is of no moment since the result in construction would still in no way disclose or suggest the presently claimed invention.

Furthermore, whether or not Sullivan discloses a circuit for adjusting an output impedance and whether or not one of ordinary skill in the art would consider modifying Fontanella, Hanks, or Murray is of no moment since the result in construction would still in no way disclose or suggest the presently claimed invention.

Applicants respectfully submit that Hanks, Murray, and Sullivan do not relate to mass storage devices.

Hanks relates to a control system for an airbag.

Murray relates to an admittance circuitry. While Sullivan relates to a power supply for an electrical mechanical device.

Liu does not relate to a mass storage device.

These references do not relate to a piezo element in a milli-actuator device and a mass storage device.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-8 and 10-42 under 35 U.S.C. § 103 and 35 U.S.C. § 112 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'WDS', is written over the printed name of the attorney.

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APPENDIX

Claim 1 (original): An integrated circuit for providing drive signals to a piezo element of a milli-actuator device in a mass data storage device, comprising:

a driving circuit for selectively driving said piezo element in either a voltage mode or a charge mode; and

a circuit for compensating said driving circuit for a variable number of piezo elements in a charge mode of operation and providing a compensating feedback signal in a voltage mode of operation.

Claim 2 (original): The integrated circuit of claim 1 wherein said circuit for compensating said driving circuit for a variable number of piezo elements in a charge mode of operation comprises a circuit for adjusting an output impedance of at least a portion of said driving circuit.

Claim 3 (previously presented): The integrated circuit of claim 2 wherein said circuit for adjusting an output impedance of at least a portion of said driving circuit comprises a plurality of resistance providing elements that are selectively switched into the circuit.

Claim 4 (original): The integrated circuit of claim 3 wherein said resistance providing elements comprise a plurality of series connected MOSFET devices.

Claim 5 (original): The integrated circuit of claim 3 wherein said resistance providing elements comprise a plurality of integrated resistors.

Claim 6 (original): The integrated circuit of claim 1 further comprising a circuit for containing command data to specify a mode of operation of said integrated circuit.

Claim 7 (previously presented): The integrated circuit of claim 6 further comprising circuitry for configuring said integrated circuit to operate in a voltage mode or a charge mode in response to said command data to specify a mode of operation of said integrated circuit.

Claim 8 (previously presented): The integrated circuit of claim 6 wherein said integrated circuit further comprising circuitry for configuring a parameter of said integrated circuit to compensate for said number of piezo element devices.

Claim 9 (cancelled)

Claim 10 (original): An integrated circuit for providing drive signals to a piezo element of a milli-actuator device in a mass data storage device, said piezo element including a variable number of piezo element devices, comprising:

- a Class A amplifier connected to receive input signals for controlling said piezo element;

- a Class AB amplifier connected to receive an output from said Class A amplifier to selectively provide either current mode driving signals or voltage mode driving mode signals to said piezo element; and

- a circuit for compensating said integrated circuit,

- wherein in a charge mode of operation, said circuit for compensating said integrated circuit selectively compensates said Class A amplifier for a variable number of piezo element devices,

- and wherein in a voltage mode of operation, said circuit for compensating said integrated circuit provides a compensating feedback signal.

Claim 11 (original): The integrated circuit of claim 10 wherein said circuit for compensating said driving circuit for a variable number of piezo elements comprises a circuit for adjusting an output impedance of said Class A amplifier.

Claim 12 (original): The integrated circuit of claim 11 wherein said circuit for adjusting an output impedance of at said Class A amplifier comprises a plurality of resistance providing elements that are selectively connected in said Class A amplifier.

Claim 13 (original): The integrated circuit of claim 12 wherein said resistance providing elements comprise a plurality of series connected MOSFET devices.

Claim 14 (original): The integrated circuit of claim 12 wherein said resistance providing elements comprise a plurality of integrated resistors.

Claim 15 (original): The integrated circuit of claim 10 further comprising a circuit for containing command data to specify a mode of operation of said integrated circuit.

Claim 16 (original): The integrated circuit of claim 15 further comprising circuitry for configuring said integrated circuit to operate in a voltage mode or a current mode in response to said command data to specify a mode of operation of said integrated circuit.

Claim 17 (original): The integrated circuit of claim 15 wherein said piezo element has a number of piezo element devices, and further comprising circuitry for configuring a parameter of said integrated circuit to compensate for said number of piezo element devices.

Claim 18 (original): The integrated circuit of claim 17 wherein said parameter is an impedance of at least a portion of said integrated circuit.

Claim 19 (previously presented): A method for providing drive signals to a piezo element of a milli-actuator device in a mass data storage device, including a variable number of piezo element devices, comprising:

selectively driving said piezo element in either a voltage mode or a charge mode;
and

compensating said driving circuit for said variable number of piezo element devices in a charge mode of operation and providing a compensating feedback signal in a voltage mode of operation.

Claim 20 (original): The method of claim 19 wherein said compensating said driving circuit for a variable number of piezo element devices in a charge mode of operation comprises adjusting an output impedance of at least a portion of said driving circuit.

Claim 21 (previously presented): The method of claim 20 wherein said adjusting an output impedance of at least a portion of said driving circuit comprises selectively switching a plurality of resistance providing elements into the circuit.

Claim 22 (original): The method of claim 21 wherein said selectively connecting a plurality of resistance providing elements into the circuit comprises selectively connecting a plurality of series connected MOSFET devices into the circuit.

Claim 23 (original): The method of claim 21 wherein said selectively connecting a plurality of resistance providing elements into the circuit comprises selectively connecting a plurality of resistors into the circuit.

Claim 24 (original): The method of claim 19 further comprising containing command data to specify a mode of operation of said integrated circuit.

Claim 25 (previously presented): The method of claim 24 further comprising configuring said integrated circuit to operate in a voltage mode or a charge mode in response to said command data.

Claim 26 (original): The method of claim 25 wherein said configuring a parameter of said integrated circuit to compensate for said number of piezo element devices comprises configuring an impedance of at least a portion of said integrated circuit.

Claim 27 (original): An integrated circuit for providing drive signals to a piezo element of a milli-actuator device in a mass data storage device, said piezo element including a variable number of piezo element devices, comprising:

means for selectively driving said piezo element in either a voltage mode or a charge mode; and

means for compensating said driving circuit for said variable number of piezo element devices in a charge mode of operation and providing a compensating feedback signal in a voltage mode of operation.

Claim 28 (original): The integrated circuit of claim 27 wherein said means for compensating said driving circuit for a variable number of piezo element devices in a charge mode of operation comprises means for adjusting an output impedance of at least a portion of said driving circuit.

Claim 29 (previously presented): The integrated circuit of claim 28 wherein said means for adjusting an output impedance of at least a portion of said driving circuit comprises means for selectively switching a plurality of resistance providing elements into the circuit.

Claim 30 (original): The integrated circuit of claim 29 wherein said means for selectively connecting a plurality of resistance providing elements into the circuit comprises means for selectively connecting a plurality of series connected MOSFET devices into the circuit.

Claim 31 (original): The integrated circuit of claim 29 wherein said means for selectively connecting a plurality of resistance providing elements into the circuit comprises means for selectively connecting a plurality of resistors into the circuit.

Claim 32 (original): The integrated circuit of claim 27 further comprising means for containing command data to specify a mode of operation of said integrated circuit.

Claim 33 (original): The integrated circuit of claim 32 further comprising means for configuring said integrated circuit to operate in a voltage mode or a current mode in response to said command data.

Claim 34 (original): The integrated circuit of claim 33 wherein said means for configuring a parameter of said integrated circuit to compensate for said number of piezo element devices comprises means for configuring an impedance of at least a portion of said integrated circuit.

Claim 35 (previously presented): A mass data storage device, comprising:
an integrated circuit for providing drive signals to a piezo element of a milli-actuator device in a mass data storage device, said integrated circuit including:
a driving circuit for selectively driving said piezo element in either a voltage mode or a charge mode; and
a circuit for compensating said driving circuit for a variable number of piezo elements in a charge mode of operation and providing a feedback signal in a voltage mode of operation.

Claim 36 (original): The mass data storage device of claim 35 wherein said circuit for compensating said driving circuit for a variable number of piezo elements in a charge mode of operation comprises a circuit for adjusting an output impedance of at least a portion of said driving circuit.

Claim 37 (previously presented): The mass data storage device of claim 36 wherein said circuit for adjusting an output impedance of at least a portion of said driving circuit comprises a plurality of resistance providing elements that are selectively switched into the circuit.

Claim 38 (original): The mass data storage device of claim 37 wherein said resistance providing elements comprise a plurality of series connected MOSFET devices.

Claim 39 (original): The mass data storage device of claim 37 wherein said resistance providing elements comprise a plurality of integrated resistors.

Claim 40 (original): The mass data storage device of claim 35 further comprising a circuit for containing command data to specify a mode of operation of said integrated circuit.

Claim 41 (original): The mass data storage device of claim 40 further comprising circuitry for configuring said integrated circuit to operate in a voltage mode or a current mode in response to said command data to specify a mode of operation of said integrated circuit.

Claim 42 (previously presented): The mass data storage device of claim 40 wherein said mass data storage device further comprising circuitry for configuring a parameter of said integrated circuit to compensate for said number of piezo element devices.

Claim 43 (cancelled)